Device Scaling Physics and Channel Velocities in AlGaN/GaN HFETs: Velocities and Effective Gate Length

Yuh-Renn Wu, *Student Member, IEEE*, Madhusudan Singh, *Member, IEEE*, and Jasprit Singh

***Abstract*—This paper addresses scaling issues in AlGaN/GaN heterojunction field-effect transistors (HFETs) using ensemble Monte Carlo techniques. For gate lengths below 0.25 μm, f_T values are known not to scale linearly with the inverse gate length. The authors' simulations show this to be due to an increasing difference between the lithographic gate length and the effective gate length as the devices shrink. The results for AlGaN/GaN are compared with $In_{0.52}Al_{0.48}$-$In_{0.53}Ga_{0.47}$As-InP devices, and the authors found that the limiting role of velocity overshoot and depletion region spread causes the GaN HFETs to have a peak f_T of $\sim$ 220 GHz compared to $\sim$ 500 GHz for InGaAs devices.**

***Index Terms*—AlGaN, effective gate length, GaN, heterojunction field-effect transistors (HFETs), InGaAs, InP, recessed gate, scaling, III-V nitrides.**

I. Introduction

OVER THE LAST several years, AlGaN/GaN HFETs have emerged as a very promising technology for microwave high-frequency and high-power applications. AlGaN/GaN HFETs have been demonstrated with a unity current gain frequency f_T of as high as 152 GHz at $V_{DS} = 6$ V and an f_{max} as high as 230 GHz [1] at $V_{DS} = 18$ V. An experimental picture of the scaling of f_T with gate length has emerged over the last few years [1]–[6]. Cutoff frequencies range from $\sim$ 86 GHz for a 0.25-μm gate-length [4] device to 152 GHz for a 60-nm gate-length [2] device, and 153 GHz for a 100-nm gate length [1] with an $In_{0.10}Ga_{0.90}$N back barrier. It has been suggested that due to the high optical phonon scattering rates, built up of optical phonons causes high scattering rates and, thus, suppresses carrier velocities. However, Monte Carlo studies [7] and latest experimental reports on very high-frequency devices suggest that this may not occur. Recently, average velocities in the channel have been extracted through measurement and have reached $1.6 \sim 2.0 \times 10^7$ cm/s [1], [4]. Several questions need to be addressed to fully exploit the AlGaN/GaN HFET technology. These include the following.

1) What is the source of sublinear f_T dependence on inverse gate length?
2) Is the velocity in GaN channel suppressed below the values expected from Monte Carlo studies?
3) What is the highest cutoff frequency possible in AlGaN/GaN HFETs?
4) How do scaling issues in AlGaN/GaN devices compare with other high-frequency devices?

In this paper, we address the issues raised above. In particular, we examine the role of the effective gate length L_{eff} [8] versus lithographic gate length L_G and nonlocal transport (i.e., velocity-overshoot effects). We found that the ratio L_{eff}/L_G increases from 1.5 to 6 as L_G changes from 0.25 to 0.03 μm. This ratio also depends upon the device bias conditions. The high ratio usually causes the parasitic and drain delays [9], [10]. The impact of L_{eff} on the device performance and average electron velocities is studied. Finally, we compare the GaN-device results to $In_{0.52}Al_{0.48}$As-$In_{0.53}Ga_{0.47}$As-InP HEMTs.

II. Formalism

In this section, we provide a brief description of the basic formalism for studying the scaling issues.

1) We use our two-dimensional (2-D) Poisson and drift-diffusion finite element (FEM) solver [11] to obtain the current–voltage $(I-V)$ curves, charge distribution, and electric field along the channel.
2) Use the quasi-Fermi levels obtained from the 2-D-Poisson and drift-diffusion solver to solve Schrödinger and Poisson equations to obtain the wave function and 2-D confined energy level for the different points.
3) Employ the 2-D and three-dimensional (3-D) multivalleys (Γ, L, and $U-M$) ensemble Monte Carlo (EMC) method and electric-field (E_x) profile to simulate the spatial velocity of electrons along the channel [7].
4) Use the spatial velocity of the electrons obtained from EMC as the new mobility model and feed it back to 2-D-Poisson and drift-diffusion solver to solve the equation self-consistently [12].

The 2-D-Poisson and drift-diffusion equation solvers basically solve the Poisson, drift-diffusion, and continuity equations self-consistently with FEM. Shockley–Read–Hall

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recombination/generation mechanism is included in the continuity equation. The effects of polarization at AlGaN/GaN interface are included through a charge-control model. The detailed formalism for solving the Poisson and drift-diffusion equations with FEM can be found in the recent work [11].

From the 2-D-Poisson and drift-diffusion solver, we obtain the field profile, quasi-Fermi level, and charge distribution in the channel. However, the Schrödinger equation can only be solved in perpendicular y-direction to obtain the confined state in the channel. Therefore, we solve the one-dimensional (1-D) Schrödinger equation and Poisson equation at each x point to obtain the wave function and the 2-D confined energy level for different x points. The scattering rate at each point x under the channel is calculated. Then, we use the EMC method [7] to simulate the electron velocity through the electric field $E_x(x)$. For short-channel effects, the E_y component mainly influences the charge density especially near the drain depletion region. This effect is already taken into account by applying different scattering rates at different points, as mentioned before. We carry out the 2-D and 3-D EMC method with 500 000 electrons for this structure. The statistical electron velocities and energy along different positions of the channel are then recorded and averaged. The MC process takes the following scattering mechanisms into account: 1) polar optical-phonon absorption and emission; 2) acoustic phonon scattering; 3) interface roughness scattering; 4) equivalent and nonequivalent intervalley scattering; 5) alloy scattering; and 6) charged dislocation scattering. Typical parameters from literature are used [13], [14].

For the first iteration, the spatial velocity of electron is obtained from the electric field calculated from the steady-state mobility model. However, for the short-channel devices, the steady-state mobility model may not work well due to the velocity-overshoot effects. The electric-field component $E_x(x)$ obtained from the steady-state mobility model may not be correct in such short-channel devices. For a better accuracy, we need to couple the EMC into 2-D-Poisson and drift-diffusion solver to solve the equation self-consistently. Therefore, the spatial velocity and the old $E_x(x)$ in the channel are then used as the new mobility model for the 2-D-Poisson and drift-diffusion solver to obtain the new electric-field $E_x(x)$ and charge-distribution profile. Then, the previous steps are repeated to solve the equations self-consistently. With these iteration steps, we can obtain the spatial electron velocity accurately.

III. Results

In our simulations, we address several issues: 1) the effective gate length in the channel as determined by a gate charge control versus the lithographic length; for this, we examine the charge distribution in the channel and its variation with bias conditions; 2) the velocity distribution in the channel; 3) the effective velocity in the channel using the effective gate length and how it compares to the velocity if we were to assume the lithographic gate length and transit time; and 4) cutoff frequency determined by the effective transit time that includes the effects of depletion length on the source and drain side.

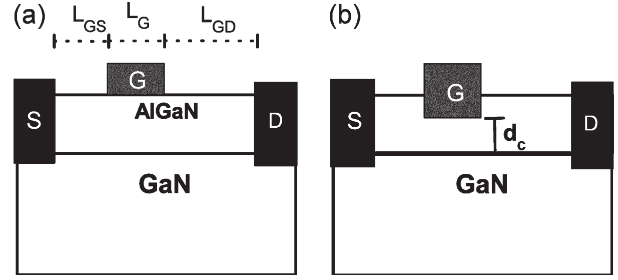

Fig. 1. Schematic cross section of AlGaN/GaN HEMT structures. (a) Device without recessed gate. (b) Device with recessed gate. L_{GS} is 0.35 μm. The total channel length $(L_{\mathrm{GS}} + L_G + L_{\mathrm{GD}})$ is 1.6 μm.

Fig. 1 shows the schematic cross section of the nitride HFET. The $Al_{0.35}Ga_{0.65}N$ barrier layer thickness is 290 Å. The temperature is 300 K and L_{GS} is 0.35 μm in all cases, unless otherwise specified. The total channel length $(L_{\mathrm{GS}} + L_G + L_{\mathrm{GD}})$ is 1.6 μm. For very short gate lengths $(< 0.15\ \mu\mathrm{m})$, the gate loses control over the channel unless it is recessed. Thus, we examine the recessed-gate device as well. Fig. 1(b) shows a schematic of the recessed-gate case. The gate-to-channel distance d_c is 100 Å for our recessed-gate studies.

Fig. 2(a) shows the calculated charge distribution along the channel for different gate biases for a 0.1-μm gate-length device. The actual size and position of the real gate is labeled in Fig. 2(a). The drain bias V_{DS} is 10 V. The estimated effective gate length is also marked in the figure for the gate bias $V_{\mathrm{GS}} = -5$ V. The effective gate length is determined by the length of the depletion region for different gate biases individually. The increased effective gate length σ on the source side can be explained as being due to the fringing effect at the edges of the gate capacitor formed between the gate and the channel region. This effect can be reduced by decreasing the gate-to-channel distance and increasing the aspect ratio of gate length to gate-to-channel distance. However, for the smaller $d_c (< 100$ Å$)$, there might be tunneling-related gate-leakage problems [15] in the system. The threshold voltage of the recessed gate will shift to ~ -1.5 V for $d_c = 10$ nm, and the device will need to operate at positive gate voltage to prevent the channel from becoming fully depleted. However, our studies [15] show that when the gate bias is larger than 1.0 V, the leakage current density is higher than 10^8 A/cm^2. Therefore, the range of recessed thickness is limited and modulation doping in the AlGaN layer may be needed to increase the charge density in the channel. The increased effective gate length at the drain end δ is much larger than the value at the source end. This is due to the additional strong horizontal electric field E_x induced by the drain bias. As the drain bias increases, the larger E_x-to-E_y ratio leads to a larger asymmetric channel depletion length δ. For zero drain bias, L_{eff} reduces to $L_g + 2\sigma$, which is the fundamental limiting value of L_{eff}.

Fig. 2(b) shows the velocity calculated by EMC method. It is apparent that there is a velocity-overshoot effect at the end of a 0.1-μm channel. However, the overshoot region is small. The average velocity v_{ave} under the real gate region is very high $(\sim 2.7 \times 10^7$ cm/s$)$. However, due to the increase of the L_{eff}, v_{ave} in the effective gate-length region is reduced to $\sim 1.6{-}2.0 \times 10^7$ cm/s, which is closer to the recently reported

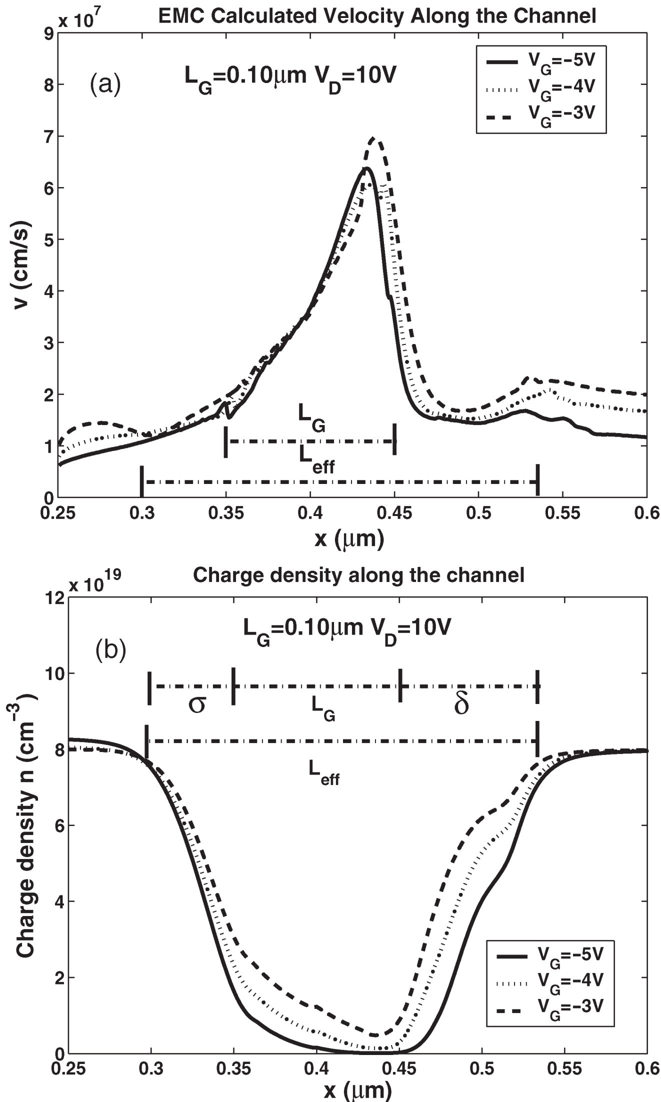

Fig. 2. (a) Charge distribution in the channel with different gate voltages. L_G is 0.1 μm and V_D is 10 V. The label of effective gate length in the figure is marked for $V_{\rm GS} = -5$ V. (b) Velocity along the channel calculated by EMC method.

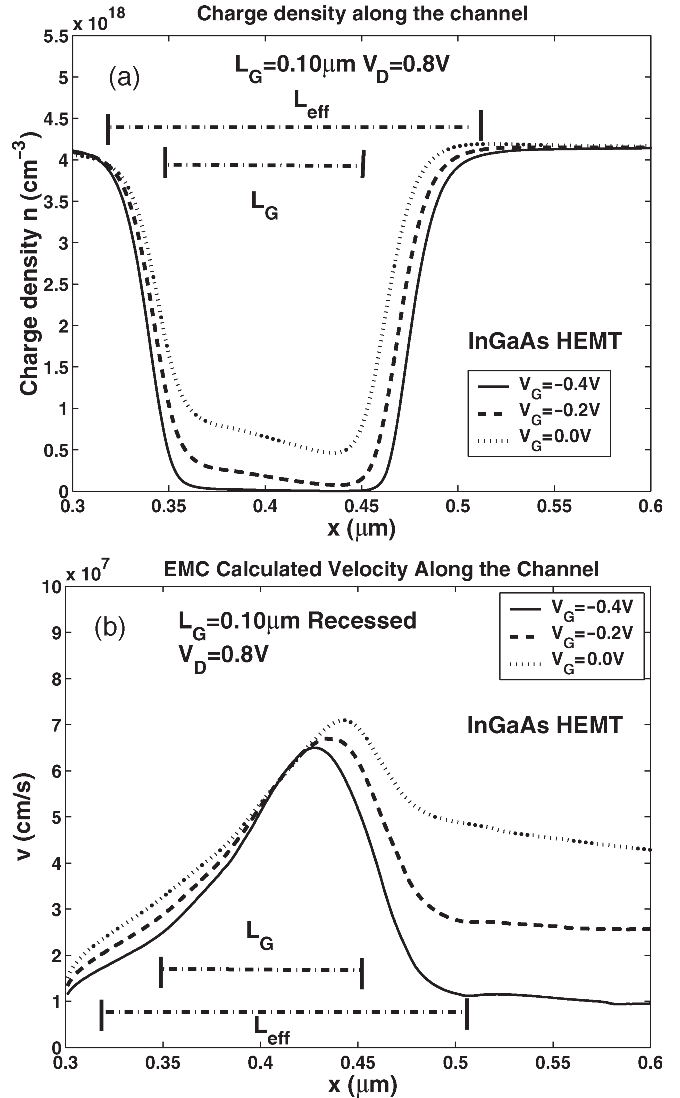

Fig. 3. (a) Charge distribution in the channel with different gate voltages for InAlAs/InGaAs HEMTs. L_G is 0.1 μm and V_D is 0.8 V. (b) Velocity along the channel calculated by EMC method. The velocity-overshoot region is much larger compared to GaN HFETs.

average intrinsic velocity 1.6×10^7 cm/s by Palacios *et al.* [1]. It may be noted that for the experimental extracted velocity, the depletion length δ at $V_{\rm DS} = 0$ V is assumed to be zero, which is not correct especially for short gate devices. Therefore, the velocity in the channel is usually underestimated by neglecting the depletion region 2σ. As shown in Fig. 2(a), $2\sigma \sim 0.08$ μm, approximately 90% of the real gate length for a gate length equal to 0.1 μm. By considering this effect, the estimated experimental velocity may be 1.8 times larger than the reported one. The experimentally estimated velocity under the real gate region should be $\sim 2.88 \times 10^7$ cm/s, which is very close to our simulation. Using the simulation results, we can calculate the maximum extrinsic f_T by modifying the ideal intrinsic f_T equation

$$f_T = \frac{1}{2\pi t_r} = \frac{v_{\rm ave}}{2\pi L_{\rm eff}} \tag{1}$$

where L_G is replaced by $L_{\rm eff}$, and $v_{\rm ave}$ is the average velocity of electron in the effective gate region. Due to the increase of $L_{\rm eff}$ and the decrease of $v_{\rm ave}$ in the effective gate region, the increase of f_T with the decrease of the gate length is not as large as expected, and velocity-overshoot effect is compensated by the increase of $L_{\rm eff}$. The calculated maximum f_T for $L_G = 0.1$ μm is 147 GHz at $V_D = 10$ V, which is very close to the reported 152 GHz by Palacios *et al.* [1].

It is useful to compare the AlGaN/GaN-based devices with InGaAs-InP devices. InGaAs devices have high mobilities and velocity-field relations that are quite different. Fig. 3 shows the calculated charge distribution and velocity along the channel of $In_{0.52}Al_{0.48}As$-$In_{0.53}Ga_{0.47}As$-InP HEMTs using the EMC method. The dimension of InGaAs HEMTs is the same as GaN HFETs. A 10-Å δ doping is assumed at 50 Å above the interface of InAlAs/InGaAs. The gate is recessed 140 Å and d_c is 150 Å. The gate length of InGaAs HEMTs is 0.1 μm, and the $V_{\rm DS}$ is 0.8 V. Comparing the nitride HFETs, there are several differences. The velocity-overshoot effect is stronger and exists in the whole gate region compared to the nitride HFETs.

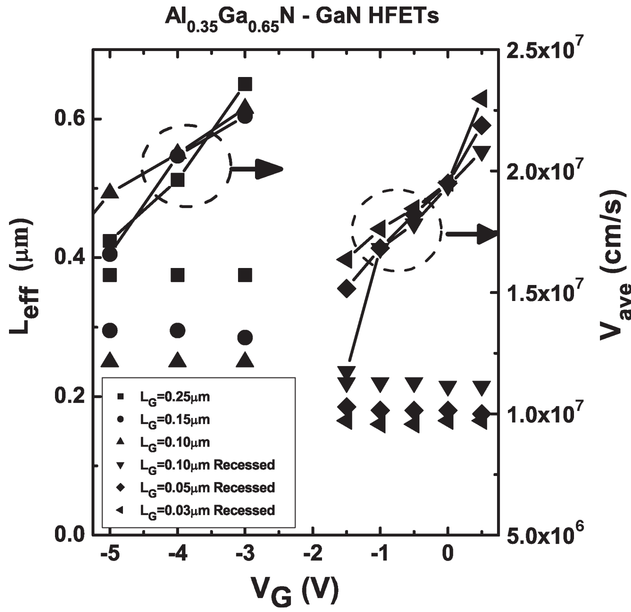

Fig. 4. L_{eff} and v_{ave} in the effective gate region versus gate voltage. The symbols with a line through them represent v_{ave} and the symbols without a line represent L_{eff}. The two sets of results are for unrecessed- and recessed-gate cases. The drain bias V_D is 10 V. It may be noted that for a recessed-gate device, the device operates at a larger gate bias.

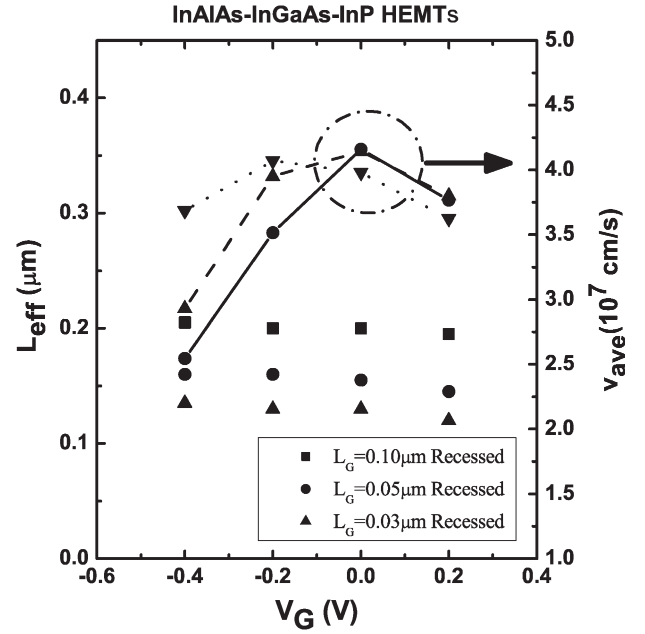

Fig. 5. L_{eff} and v_{ave} in the effective gate region versus gate voltage of $\text{In}_{0.52}\text{Al}_{0.48}\text{As-In}_{0.53}\text{Ga}_{0.47}\text{As-InP}$ HEMTs. The symbols with a line through them represent v_{ave} and the symbols without a line represent L_{eff}. The drain bias V_D is 0.8 V. For $L_G \leq 0.1$ μm, the recessed gate is essential to pinchoff the device.

The average velocity in the effective gate region is approximately 3.8×10^7 cm/s, which is approximately 1.8 times larger than the GaN HFET. The simulation shows that the effective gate length is strongly affected by the sheet-charge density in the channel. However, although the GaN HFET has a larger sheet-charge density $(\sim 1.4 \times 10^{13}\ \text{cm}^{-2})$ than the InGaAs HEMT $(\sim 2.5 \times 10^{12}\ \text{cm}^{-2})$, the depletion length of InGaAs HEMTs is shorter due to the much smaller operation V_{DS} ($\sim$ 0.8 V compared to the 10 V of GaN HFETs).

Fig. 4 shows the estimated L_{eff} and v_{ave} for different gate-bias and gate-length values. For the nonrecessed-gate cases, the f_T maximum occurs approximately for $V_G = -3 \sim -4$ V and for the recessed cases, the f_T maximum occurs approximately at $V_G = 0$ V. As shown in the Fig. 4, the increase of gate bias increases v_{ave} in the channel. For most cases, f_T increases as the gate bias increases. However, with larger gate bias, the stronger self-heating effects due to the increase of current and nonlinear gate source resistance [11] may lead to the decrease of f_T. Our simulations show that recessed gate is needed when gate length is smaller than 0.15 μm. As shown in Fig. 4, the effective gate length decreases as the gate is recessed for $L_G = 0.10$ μm. The gate loses the control of the channel charge for the nonrecessed-gate devices, and the channel is hard to pinchoff. This is due to the low-aspect ratio of the gate length to gate-to-channel distance so that the gate behaves more like a point source rather than a field plate. It may be noted that using the p-type doping or employing a quantum well [4] would enhance the chance of device pinchoff. For the 30-nm recessed-gate case, we use a d_c value of 100 Å. However, the gate does not have a good control over the channel, and a smaller d_c value is needed. As mentioned earlier, the decrease of d_c leads to a larger gate leakage and additional design work is required to reduce that [15].

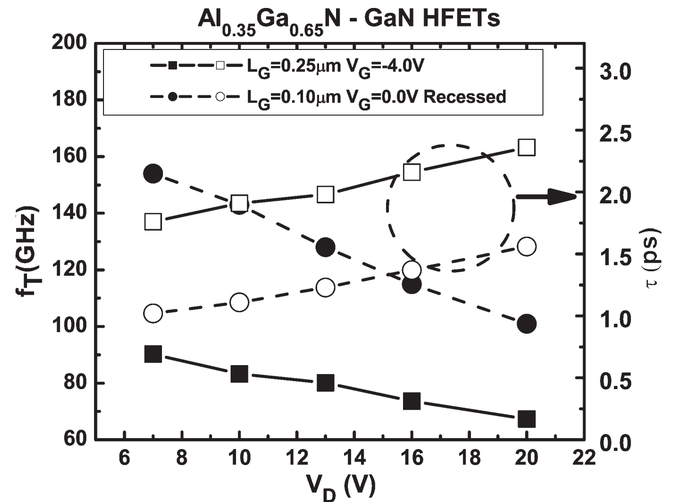

Fig. 6. f_T and transit time τ versus drain voltage V_D for different gate length. The filled symbols and hollow symbols represent the f_T and transit time τ, respectively.

Fig. 5 shows the estimated L_{eff} and v_{ave} for the InGaAs HEMTs. As mentioned earlier, the V_{DS} of the InGaAs HEMT is much smaller than the GaN. The effective gate length is scaled down more linearly as the real gate shrinks. When the gate length continues to decrease, the effective gate length also decreases. Therefore, the device has a much better scalability. For the InGaAs HEMT, the recessed gate is essential when the gate length is smaller than 0.1 μm.

Fig. 6 shows the unity current gain cutoff frequency and the transit time versus the drain voltage. It is known that AlGaN/GaN devices do not suffer a large reduction in f_T when the drain bias is increased (contrary to GaAs or InGaAs-based HEMTs). However, as shown in Fig. 6, larger drain bias

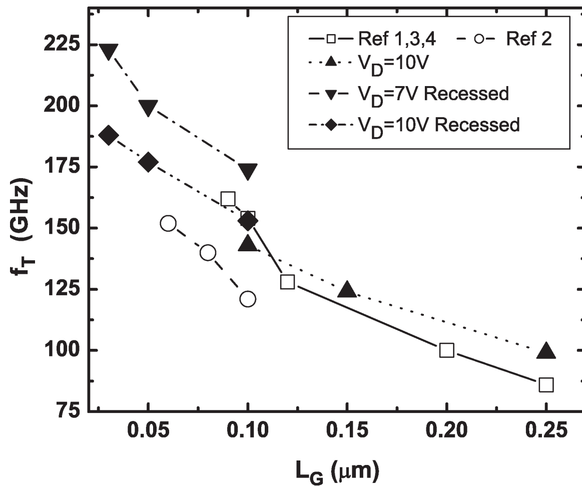

Fig. 7. Comparison of maximum f_T between simulations and experimental results. The experimental results are from different references [1]–[4].

still leads to a larger depletion region at the drain side and decrease of f_T, especially for a smaller gate length, where f_T is mainly dominated by the effective gate length. But due to a much larger sheet-charge density (ten times larger than GaAs HEMTs and 5 times larger than InGaAs-based HEMTs), the decrease rate of f_T is much smaller compared to GaAs or InGaAs-based HEMTs. The simulation also shows that for the same drain-bias condition, the depletion length of GaN is much smaller than InGaAs devices. Therefore, AlGaN/GaN HFETs have a better performance for high-voltage applications. The calculated drain delay for the $L_G = 0.10$ μm, recessed HFET, is 0.042 ps/V at $V_G = 0$ V and the drain delay for the $L_G = 0.25$ μm, HFET is 0.045 ps/V at $V_G = -4$ V.

Fig. 7 shows the maximum f_T obtained from the experiments and calculated results. Maximum f_T of GaN is calculated for $V_{DS} = 7$ V and 10 V. The simulation shows a good agreement with the maximum f_T reported by experiments [1], [2], and [4]. In comparing the recessed-gate and nonrecessed-gate cases, we find that the increase of f_T is not very significant. However, a recessed gate allows us to turn the device OFF since for short channels (≤ 0.10 μm), the gate loses control on the channel if a recessed structure is not employed. These results suggest that the maximum achievable f_T for nitrides would be close to 220 GHz $\pm$5%, errors being due to the estimation errors in $L_{\rm eff}$ at $V_{DS} = 7$ V. It is noted that most GaN HFETs are passivated at the AlGaN surface in order to remove the surface-trap effects. In our simulation, the effect of passivation layer, such as SiN, is not considered. The passivated layer might increase the effective gate length significantly by increasing the drain-gate and source-gate capacitance. Growing a thinner passivation layer [1] and using a smaller dielectric constant materials to passivate the surface might improve the device performance.

Fig. 8 shows the maximum f_T of InGaAs HEMTs obtained from experiments [16], [17] and calculated results. Maximum f_T is estimated to be around 500 GHz at $V_{DS} = 0.8$ V, which shows a very good agreement with the experimental reports. The reasons for higher f_T in InGaAs are the smaller effective gate length due to smaller V_{DS} and the much stronger velocity-

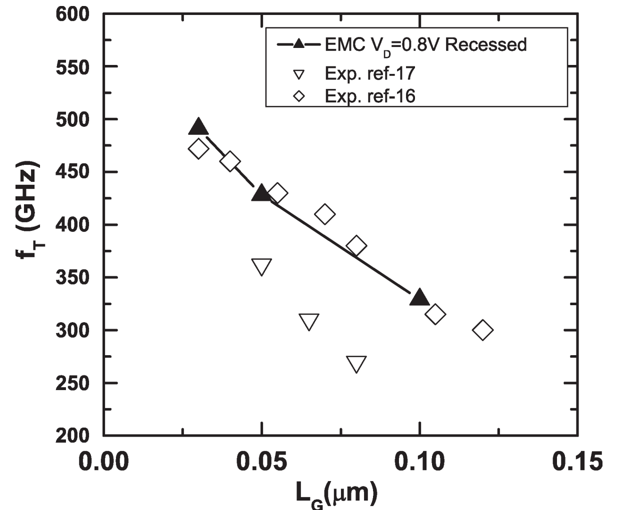

Fig. 8. Comparison of simulations and experimental results for maximum f_T versus L_G for $In_{0.52}Al_{0.48}As$-$In_{0.53}Ga_{0.47}As$ HEMTs. The experimental results are from different references [16], [17]. The drain bias V_D is 0.8 V as indicated in the legend.

overshoot effect. Due to the much larger effective mass and the appearance of the peak velocity at very high-electric-field region ($\sim 1.3 \times 10^5$ V/cm), the GaN HFETs cannot be operated at lower drain-bias condition (i.e., linear region instead of saturation region). Therefore, the way to improve the device performance would be to either increase the sheet channel charge density by modulation doping or shift to InGaN system [18], which has a smaller effective mass, larger sheet-charge density, and a higher peak electron velocity.

IV. Conclusion

In this paper, theoretical results for $L_{\rm eff}$ and $v_{\rm ave}$ in the III-V nitride HFETs are presented. The comparison between the GaN and InGaAs is also studied. The simulations show that the degree of overshoot effects and effective gate length play a very important role of limiting the device performance. The simulations shed light on the difficulty of reducing parasitics and drain delay in the AlGaN/GaN device. The modified maximum extrinsic f_Ts of GaN HFETs and InGaAs HEMTs are predicted and the results are in very good agreement with the experiments. The maximum achievable f_T for GaN-based HFETs is predicted to be around 220 GHz. Possible improvements in the f_T value could arise from the use of InN channels [14], although the device may not be able to generate high power.

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