Effect of image charges in the drain delay of AlGaN/GaN high electron mobility transistors

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The drain delay in AlGaN/GaN submicron high electron mobility transistors (HEMTs) accounts for almost 25% of the total electron delay. This long delay significantly limits the maximum frequency performance and linearity of these devices. This paper studies the origin of this important delay assuming that it is inversely proportional to α, a parameter related to how injected channel electrons image at different contacts in the HEMT. Through analysis and two-dimensional simulations, we have found that α equals 3 in a standard HEMT. This value has been confirmed experimentally through the coupling of Monte Carlo simulations and drain delay measurements. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2889498]

AlGaN/GaN high-electron mobility transistors (HEMTs) have recently shown an outstanding performance. In only 15 years, GaN-based transistors have evolved tremendously from the initial devices with less than 40 mA/mm of output current and virtually no high frequency performance[1] to worldwide commercialization as power amplifiers in the *S* and *X* bands.[2] The excellent intrinsic properties of nitride semiconductors such as large sheet charge density ($\sim 1\times 10^{13}$ cm^{-2}), high peak electron velocity ($\sim 2.5\times 10^{7}$ cm/s), high breakdown field strength ($\sim$3 MV/cm), and good thermal conductivity ($>$1.5 W/cm K) make them one of the best options for solid state power amplifiers.

One of the new challenges in GaN electronics is to increase their frequency of operation to millimeter and submillimeter wave frequencies. To achieve this goal, improved growth in combination with the introduction of new device structures such as InGaN (Ref. 3) and AlGaN back barriers[4] and catalytic-chemical vapor deposition SiN gate-insulating and passivation layers[5] have been recently reported. These new structures have allowed devices with a current gain cutoff frequency (f_T) in excess of 150 GHz and a maximum oscillation frequency ($f_{\max}$) of 230 GHz in AlGaN/GaN HEMTs with a gate length of 100 nm.[3] However, in spite of these excellent results, nitride devices are still far from their theoretically expected maximum performance.

The operating frequency of a HEMT is inversely proportional to the total delay of the carriers across the transistor (τ_{total}). Following the analysis of Moll *et al.*, τ_{total} can be divided into three different components: intrinsic delay (τ_{int}), channel charging delay (τ_{channel}), and drain delay (τ_{drain}).[6] τ_{int} is the time taken by the electrons to cross the channel region under the gate, τ_{channel} is the time needed to charge and discharge the parasitic capacitances, and τ_{drain} is the time required by the electrons to cross the depletion region induced at the drain side of the gate. τ_{int} decreases when scaling down the device dimensions, however, τ_{drain} (and in less degree τ_{channel}) remains constant and ultimately limits the maximum frequency performance of these transistors [Fig. 1(a)].

Moreover, the linearity of f_T and $f_{\max}$ with drain voltage is also a critical parameter for high frequency operation. As shown in Fig. 1(b), the increase in drain voltage causes a reduction in f_T and $f_{\max}$ of more than 30% at high drain voltages. This decrease severely limits the large signal linearity of the transistor due to the associated nonlinearity of the gain. The origin of this decrease with drain voltage is commonly associated with the increase in the width of the depletion region at the drain side of the gate and, therefore, drain delays as the drain voltage increases.

In spite of the great importance of the drain delay in the performance of deep submicron devices, this delay has only been scarcely studied so far. In this letter, we have analyzed the origin of drain delay in AlGaN/GaN HEMTs to understand its contribution to the high frequency performance and to be able to engineer it in future generation devices.

From a physical point of view, the drain delay in HEMTs is the time taken by the channel electrons to cross the depletion region induced at the drain side of the gate. The transport of the negative sheet of charge formed by the channel electrons across the depletion region induces image charges in the nearby contacts and highly conductive access regions (i.e., gate contact and source and drain access regions). This image charge modifies the electric field in the depletion region, which ultimately affects the carrier transport in that region. This mechanism is similar to that in the collector-base space charge region of heterojunction bipolar transistors (HBTs) which is responsible of the collector delay in these devices (τ_c). The collector delay in HBTs has been extensively studied in the past from the current transfer function[7] and charge-control analysis.[8] These works have shown that if v_e is the scattering-limited velocity of carriers traversing the collector-base space charge region having width w, then $\tau_c = w/(2\times v_e)$. The factor of 2 in the denominator of this expression accounts for the image charge induced at both sides of the space charge region when the carriers are crossing this region.[9]

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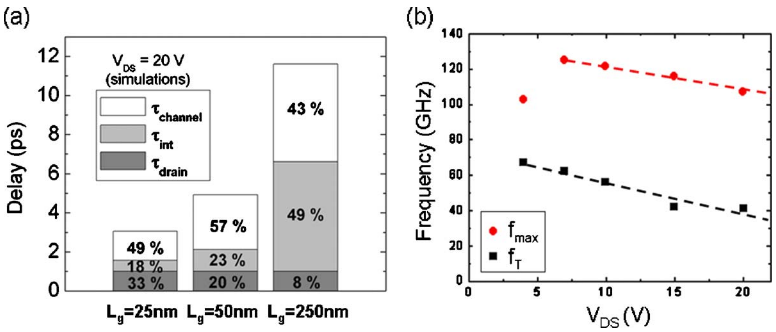

FIG. 1. (Color online) (a) Effect of the different components of the electron delay in the performance of AlGaN/GaN HEMTs with several gate lengths. (b) Variation of f_T and $f_{\max}$ with drain voltage in a typical AlGaN/GaN HEMT.

By analogy with HBTs, we define the drain delay (τ_{drain}) in HEMTs as

$$\tau_{\text{drain}} = \frac{w}{\alpha \times v_e}, \tag{1}$$

where w is the width of the depletion region, v_e is the electron velocity, and α is a constant given by the effect of image charges in the carrier transport. In HBTs, α is equal to 2.[7–9] However, the value of α has not been studied in detail in field effect transistors and several reports offer contradictory values. For example, some authors neglect the effect of image charges in the transport of electrons accross the drain depletion region and assume that α equals to 1.[10–12] Other texts, on the other hand, assume a behavior identical to the case of HBT devices and use a value of α equal to 2.[13] In this letter, we have used a combination of charge control analysis and two-dimensional (2D) simulations to calculate the value of α in HEMTs. From our work, α should have a value of 3 to accurately take into account the effect of image charges in the transport of electrons through the depletion region of a HEMT. This value has been confirmed experimentally through the coupling of Monte Carlo simulations and drain delay measurements.

Using charge control analysis in a way analog to the method used to calculate the collector delay in an HBT,[8] τ_{drain} in a HEMT can be written as

$$\tau_{\text{drain}} = \frac{dQ_{\text{inj}}}{dJ} = \frac{dQ_{\text{inj}}}{d\rho}\frac{1}{v_e} = \frac{dq_{\text{im},s}}{dq_{\text{inj}}}\frac{w}{v_e}, \tag{2}$$

where Q_{inj} is the injected charge density (C/m^2) in the depletion region, J is the current density (A/m^2) in the transistor channel, w is the width of the depletion region, ρ is the volume charge density (C/m^3) in the source region moving to the depletion region, $q_{\text{im},s}$ is the image charges induced in source access region, and q_{inj} is the total charge of the injected carriers into the depletion region. By combining Eqs. (1) and (2), we can express α as the ratio of injected charges in the depletion region to image charges in the source access region, $\alpha = dq_{\text{inj}}/dq_{\text{im},s}$.

To calculate this ratio in AlGaN/GaN HEMTs, we have run 2D simulations of the electric field in these devices using COMSOL MULTIPHYSICS 3.2 (formerly FEMLAB). The electrostatics application mode of this simulation software can simulate the electrical properties (e.g., electric field, potential, image charge densities, etc.) in dielectric materials with a fixed charge present. In this work, each contact or heavily doped access region (i.e., gate contact and source and drain access regions), 2D electron gas (2DEG) channel, and depletion region in a standard HEMT were defined with scaled conductive lines. After numerically solving the electrostatic equations, COMSOL calculates the amount of image charges at the source side of the channel ($dq_{\text{im},s}$) when injecting dq_{inj} charges into the depletion region.

To validate our model and the simulation software, the case of an HBT was simulated, as shown in Fig. 2(a). In this 2D small signal analysis, the base and collector regions are grounded and 2×10^{-8} C/m of negative charges are uniformly distributed into a 2 μm length space charge region. After redistribution of image charges, the calculated image charge at the base region is 9.87×10^{-9} C/m, which induces an α equal to 2.03, as expected in an HBT.

Figure 2(b) shows the simulated model structure for an AlGaN/GaN HEMT. The main difference between the HEMT model and the HBT model of the depletion region is the addition of a 200 nm long gate contact. The distance

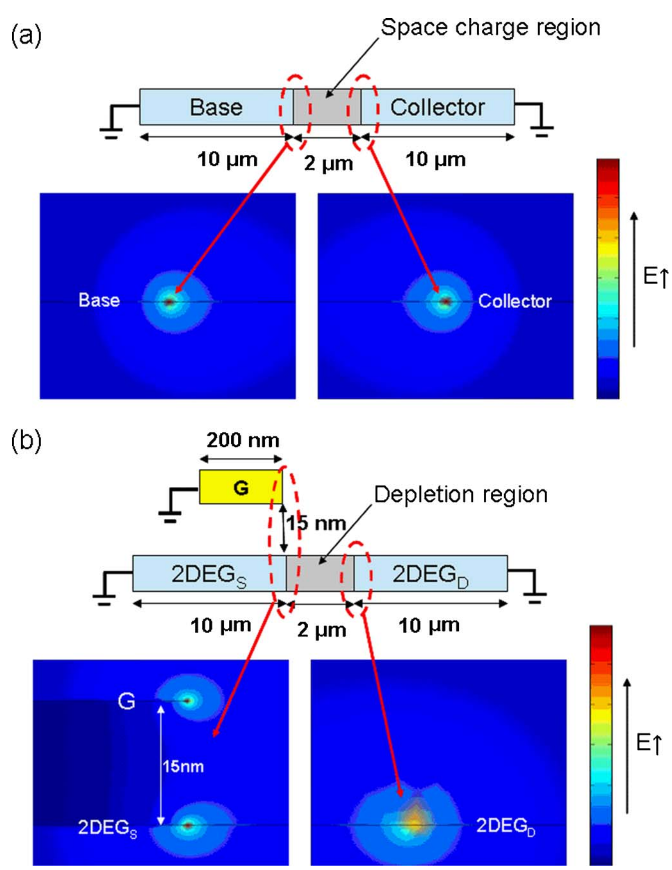

FIG. 2. (Color online) (a) Schematic illustration of simulated HBT structure model and resulting electric field after redistribution of image charges. Actual horizontal dimensions are not critical to calculate the value of α. (b) Schematic illustration of simulated HEMT structure model and resulting electric field after redistribution of image charges in the source, drain and gate contacts. $2DEG_S$ and $2DEG_D$ are 2DEGs in the source access region and drain access region, respectively.

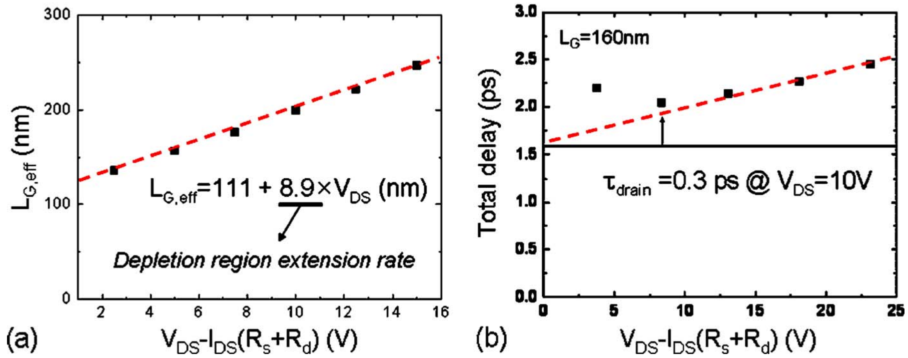

FIG. 3. (Color online) (a) Simulated effective gate length as a function of drain voltage. (b) Measurement of drain delay in a AlGaN/GaN HEMT with 160 nm gate length.

between this contact and the 2DEG is only 15 nm. In this structure, using a highly densified mesh, simulation results produce a $q_{\text{im},s}=6.65\times 10^{-9}$ C/m for a $q_{\text{inj}}=2\times 10^{-8}$ C/m, and thus, $\alpha=3$. Because of the HEMT structure, the injected charges also image at the gate metal (only 15 nm above the channel), $q_{\text{im},s}$ is about 33% less than that in the HBT case (where the charges cannot at the gate). It should be noted that no change was observed in the value of α for different widths of the depletion region. The value of α is also roughly independent (<1% change) of the distance between the gate metal and the 2DEG (5 nm–30 nm), although it is expected to decrease for longer distances.

To verify the value of $\alpha=3$, we have compared the value of the electron velocity given by Eq. (1) with the value predicted by Monte Carlo simulations in AlGaN/GaN HEMTs similar to the ones reported by Palacios *et al.*[14] The devices used in this study have a gate length of 160 nm. When applying Eq. (1), the width of the depletion region is calculated from the change in effective gate length ($L_{G,\text{eff}}$) as a function of drain voltage (V_{DS}) given by simulations of the charge density in the channel [Fig. 3(a)].[15] From these simulations, for every volt applied to the drain contact, the effective gate length increases by 8.9 nm. On the other hand, the drain delay was measured applying the analysis of Moll *et al.*[6] By measuring τ_{total} at different V_{DS} conditions, the drain delay at a given V_{DS} can be calculated as the difference between the actual measured delay and the extrapolated delay at $V_{\text{DS}}=0$ V. Figure 3(b) shows that the drain delay increases by 0.03 ps per additional volt in drain voltage. Combining both the increase of the depletion region (8.9 nm/V) and the drain delay (0.03 ps/V) with drain voltage, the electron velocity in the depletion region can be calculated by applying Eq. (1) as

$$v_e = \frac{w}{\alpha \times \tau_{\text{drain}}} = \frac{8.9\text{ nm}}{3\times 0.03\text{ ps}} \cong 1\times 10^7\text{ cm/s}. \quad (3)$$

Only $\alpha=3$ allows a good agreement with the saturated electron velocity predicted by Monte Carlo simulations.[15] Typically, the electric fields in the depletion region at the drain side of the gate are very high, in excess of 200 kV/cm. Under these values of electric field, the electron velocity is expected to saturate ($v_{e,\text{sat}}\sim 1\times 10^7$ cm/s). This value is the same as predicted by Eq. (3). The use of α different from 3 (e.g., 1 or 2) would make the experimental value to differ more than 50% from the theoretically expected value.

It should be noted that the value of α depends on how the injected channel electrons image at the different contacts. Therefore, by changing the contact structure in these devices the drain delay in a HEMT can be engineered. This is the case of field-plated or fin-field effect transistor (Fin-FET) structures. By adding a field plate structure and by varying its length and position, our simulation predicts at least a twofold improvement in the value of α; therefore improving the drain delay and linearity. These results agree with the improved linearity observed in field-plated devices.[16] The drawback of this approach is the introduction of additional gate capacitances which increase channel delay (τ_{channel}).

In summary, we have studied the effect of image charges in the drain delay of AlGaN/GaN HEMTs. Although we have focused on HEMTs, the same analysis can be applied to any other kind of FET. From our studies, in standard HEMTs, α (i.e., the proportionality factor between the drain delay and the drain depletion width) equals 3, and this value explains both theoretical predictions and experimental results of the value of the drain delay in these devices. Understanding the origin of drain delay is an important step to improve high frequency performance of AlGaN/GaN HEMTs and it opens the door to further improvements in the frequency performance of these devices by engineering how the injected channel charges image in the contacts.

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